REMARKS/ARGUMENTS

Claims 1-20 are pending in the case. The Examiner held that two publications, A Comprehensive MOSFET Mismatch Model by P. Drennan and C. McAndrew (hereinafter, "Drennan et al."), and Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design, - Ph.D. dissertation by P. Drennan (hereinafter "Drennan dissertation"), were improperly incorporated by reference into the specification. The Examiner also rejected claims 1-20 as not being enabled pursuant to 35 U.S.C. § 112(1). Finally, the Examiner rejected claims 1-20 as being obvious pursuant to 35 U.S.C. § 103 over Drennan et al., Drennan dissertation, or *McAndrew*, "Practical Modeling for Circuit Simulation article (hereinafter, "McAndrew") in view of U.S. Pat. No. 5,867,399 to Rostoker et al. (hereinafter, "Rostoker") and in the case of claim 7, in further view of U.S. Pat. No. 5,826,269 to Hussey (hereinafter, "Hussey").

Incorporation By Reference

The Examiner found that the Drennan et al. and Drennan dissertation references were improperly incorporated by reference into the specification. In response to this finding, Applicant points out that these publications were referenced to illustrate the state of the art at the time the application was filed. Accordingly, they may properly be incorporated pursuant to M.P.E.P. § 608.01(p).

112 Rejections

The Examiner rejected claims 1-20 under 35 U.S.C. § 112(1) as not being enabled because

the Mismatch Model formula recited at page 3, line 19 of the specification does not define the term, P_j. In response to this rejection, Applicant points out that consistent with Drennan et al., the term, P_j, is a variable referring to a physical process parameter such as V_{th}, T_{ox} or N_{sub}, for example. (See Drennan et al. *Abstract*). With this clarification, Applicant urges that this rejection be withdrawn.

103 Rejections

The Examiner rejected claims 1-6 and 8-20 as being obvious over the base references (Drennan et al, Drennan dissertation, and McAndrew) in view of Rostoker. In addition, the Examiner rejected claim 7 over the base references and Rostoker in further view of Hussey. Based on the claim amendments and reasons set forth herein, Applicant traverses these rejections.

For one or more references to establish a prima facie case of obviousness, it must be shown that there would have been motivation to combine the references in the manner proscribed by the Examiner and that the combined references disclose all of the limitations of the claim being rejected. (See, e.g., M.P.E.P. § 706.02(j)). While it is convenient to lump Drennan et al., the Drennan dissertation, and McAndrew together as the "base references," and use it as a primary reference together with Rostoker and Hussey, the fact still remains that four or five different references are being used to teach the elements in the claims. (Drennan dissertation and Drennan et al. are used to teach general mismatch principles; McAndrew is used to teach an editable mismatch model data library; Rostoker is used to teach a circuit simulator library and a GUI; and Hussey is used to teach the emailing of data results to a remote user.) It is generally difficult for this number of different references to properly be combinable without wrongfully picking and choosing elements from the different references. (See, e.g., *In re Fine*, 5 U.S.P.Q.2d 1596, 1600

(Fed. Cir. 1988) (One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention). The base references are directed to mismatch modeling and modeling techniques using circuit simulation. They are not, at least directly, concerned with modeling and simulation problems relating to the operational analysis of complex circuits, e.g., on an IC level. Rather, they are directed to modeling and simulating real-world problems associated with trying to manufacture equivalent transistors (e.g. for a current mirror or differential pair) within a device and modeling the expected mismatch between them based on contributing physical process parameters affecting the manufacture of the transistors. (See generally Drennan et al. *Introduction*). Rostoker, on the other hand, is concerned with providing a customizable ECAD system for designing and simulating highly complex circuits (e.g., 70,000 or more gates) at various different hierarchal levels. (See, e.g., Rostoker at col. 13, ll. 49+). Other than the fact that they relate to circuit simulation, they are actually directed to solving fairly different problems, and thus it is not clear that a skilled person would have been motivated to combine them in order to derive a mismatch modeling tool as claimed by Applicant. Hussey is even less relevant along these lines in that it relates to networked system problems and solutions; it does not even relate to programs or user interfaces for circuit modeling or simulation.

Accordingly, the cited references are not combinable as proscribed by the Examiner to establish obviousness against Applicant's claims. Regardless, however, even if combinable, they fail to teach all of the limitations of the claims, as will be pointed out in the following sections.

Independent Claims 1 and 10

Independent claims 1 and 10 have been amended to recite, in pertinent parts:

> a graphical interface to said SITMM, the graphical interface having at least one of: (a) a plurality of string-of-data input parameter fields to provide a plurality of input parameter data strings to the SITMM for generating results for at least one mismatch parameter over the plurality of input parameter data strings, and (b) a plurality of range-of-data input parameter fields to provide a plurality of input parameter ranges of data to the SITMM for generating results for at least one mismatch parameter over the plurality of input parameter ranges of data.

(Claim 1) and

> a graphical interface to said SITMM, the graphical interface having at least one field for receiving sets of data for a plurality of mismatch input parameters and providing the sets of data to the SITMM to generate mismatch output data based on the sets of mismatch input data.

(Claim 10). With these elements, claims 1 and 10 recite a system with the ability to receive multiple values, in possibly different ways (i.e., individually, in a string, in a range, and/or in a set) for each mismatch input parameter and generate mismatch output data based on the overall entered mismatch input data combination. This is valuable because it enables a user to efficiently identify input parameter combinations with favorable (e.g., reasonably reduced) mismatch results. None of the cited references, on the other hand, disclose or even suggest this capability.

As pointed out by the Examiner, Drennan et al. teaches: "[a] unique and powerful advantage of the new approach is that analysis of the contributions of the process parameters to the overall mismatch allows identification of the most important physical root causes of mismatch, which can be used to guide process diagnosis and improvement." (Office Action at page 4, last sentence *citing* Drennan *Conclusion,* sentence 4). However, this is not directed to mismatch input parameter data used to determine mismatch results for a mismatch output parameter. Rather, this

refers to breaking down an overall mismatch output parameter (e.g., drain current, I_D) into one or more constituent mismatch output parameters (e.g., process parameter components, P_j)

On the other hand, it should be pointed out that Drennan et al. does, in fact, disclose measuring drain current (an overall mismatch output parameter) over a geometric or bias parameter (which could be a type of mismatch input parameter) and shows some results of the same in Figures 1-5. (See Drennan et al. *Method* at ¶ 2; Figs. 1-5). However, neither Drennan et al. (nor the other references for that matter) disclose even a need or desire to enable a user to generate mismatch results based on different combinations of user-definable, input parameter data. Moreover, they certainly do not provide a mismatch model tool with a convenient interface for implementing the same.

Accordingly, independent claims 1 and 10, along with the remaining dependent claims, which ultimately depend from either claim 1 or 10, are not obvious over the cited references, and the rejections should thereby be withdrawn.

Claims 8, 17, and 20

In addition to the limitations previously set forth regarding claims 1 or 10, claims 8, 17, and 20 further recite a multi-dimensional plot, which is a graphical representation, of a mismatch result over several mismatch input parameters. This corresponds to a valuable feature that allows a user to readily view device mismatch data over multiple input parameters such as geometric parameters, as for example those shown for a Current Mirror mismatch versus geometry in FIG. 7. Such a graph can be used, for example, to build behavioral models for use as a look-up table, to generate trend plots over bias, geometry or temperature, and to compare devices within and across

technologies. Nothing in any of the cited references teaches or suggests this feature. Accordingly, in addition to the reasons previously set forth, the obviousness rejections to these claims should be withdrawn.

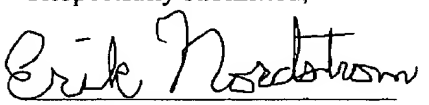
CONCLUSION

Applicant submits that all 20 claims are allowable and respectfully requests reconsideration and allowance of the application. To expedite this case, the Examiner is urged to contact Applicants' representative, Erik Nordstrom (512/238-7253) should he have any questions or recommendations.

Please send all correspondence to Freescale Semiconductor, Inc., Customer No. 23,125.

Respectfully submitted,

Date: July 26, 2004



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